REMARKS

Claims 2-6 and 8-16 are all the claims pending in the application. By this Amendment, Applicant amends claims 4 and 10 to recite the original definition of the delay time. Also, by this Amendment, Applicant amends claims 2, 3, 6, 8, 9, and 13. Claims 6 and 9 are editorially amended to fix a minor informality. In particular, in claims 6 and 9, an extra comma is deleted.

In addition, Applicant adds claims 14 and 15.

Summary of the Office Action

The Examiner objected to the Specification. In addition, the Examiner rejected claims 2-6 and 8-14 under 35 U.S.C. § 112, first paragraph. In addition, claims 2, 3, 5, 8, 9, 11, 13, and 14 stand rejected under 35 U.S.C. § 103(a) and claims 4, 6, 10, and 12 contain allowable subject matter.

Objection to the Specification

The Examiner objected to the Specification for changing the terminology "by the computer" to "in a computer" (see page 3 of the Office Action). Applicant thanks the Examiner for indicating with particularity reasons for objecting to the above noted terminology. Applicant herein amends the Specification to remove any reference to a computer.

No new matter is being added. One of ordinary skill in the art would understand that the phrase "by a computer" refers to the calculation of the delay time. That is, the delay time is calculated by the computer and not to the connection of the logic blocks. For example, the

original claim 3 is a method claim somewhat similar to the computer software product claim 10. Claim 3 clearly recites: "A method of calculating, by the use of a computer...a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks,....two logic blocks connected to each other." In other words, as is visible from the original claim 3 using a computer refers to a calculation of the delay time and not to the connection of the logic blocks. Moreover, page 20 of the specification discloses that the logic blocks are connected to each other by wires (see second full paragraph under the heading (5) "Effect of the invention" appearing on page 20). That is, the originally filed specification teaches a conventional technique of connecting the logic blocks by a wire, for example. Moreover, from the originally filed specification, it is evident that the phrase "by a computer" refers to the calculation and not to the connection of the logical blocks.

MPEP § 2163.I.B recites that "[a]n amendment to correct an obvious error does not constitute new matter where one skilled in the art would not only recognize the existence of the error in the specification, but also recognize the appropriate correction. *In re Oda*, 443 F.2d 1200, 170 USPQ 268 (CCPA 1971)". As such, the deletion of the phrase "by a computer" is clearly proper for a number of reasons detailed above. This deletion cannot be viewed as a new matter. In view of this amendment to the specification, Applicant respectfully requests the Examiner now to withdraw this objection.

Rejection under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 2-6 and 8-14 under 35 U.S.C. § 112, first paragraph. The rejections of the claims may be grouped as follows. First, claims 3-6 and 9-12 are rejected for reciting "logic blocks connected by a computer" or "logic blocks connected in a computer". Second, claims 2, 4, 8-10, 13, and 14 are rejected for reciting that plurality of values Vc comprise only of a first Vc value of a transistor connected directly to an input pin and a second Vc value of a transistor connected directly to an output pin," and for reciting a "ratios of delay time degradations." Finally, claims 4, 6, 10, and 12 allegedly contain subject matter not adequately described in the specification because the description of the derivation of expressions (5) and (6) is unclear. Applicant respectfully traverses these three groups of rejections in view of the following comments.

General Remarks

In semiconductor integrated circuits when a signal passes through transistors of the circuit a delay occurs. This delay is especially significant with N-channel transistors of small size such as Metal Oxide Semiconductors (MOS). Moreover, this delay tends to increase with the aging (degradation) of this N-channel transistor, for example, because of a hot carrier effect. In general, a circuit has a number of logic blocks and each logic block usually has a number of transistors (it may include a number of P-channel and N-channel transistors or only N-channel transistors). In each logic block, there is at least one transistor connected to an input pin and at least one transistor connected to the output pin.

A number of conventional techniques are available to calculate the aged delay time. Aged delay time is a difference in the delay time between a new circuit and a used circuit (degraded circuit). This aged delay time may be called a delay time degradation rate. One conventional technique teaches calculating the delay time degradation rate only at an input pin of each logic block. This method is a rough approximation. When accuracy is important, a technique of delay time degradation rate calculation for each transistor in the circuit is implemented. However, the number of calculation that have to be performed in this conventional technique is significant. In other words, to perform the calculations quickly, the user has to sacrifice accuracy and vise versa.

As such, it is an aspect of the present invention to provide a calculation method for calculating delay time degradation rate accurately and quickly. In particular, some exemplary experiments performed by the inventor disclosed that the transistors in the intermediate portion of the logic blocks are scarcely degraded with age.

On the other hand, inventor's experiments disclosed that it is the transistors that are directly connected to the input pin and the output pin that are most influenced by aging and age faster than the transistors in the intermediate portion. As a result, by calculating only the delay degradation rate of the transistors directly connected to the input pin and the output pin, accurate delay degradation of the circuit can be obtained at a speed faster than the conventional techniques.

In other words, in the exemplary, non-limiting embodiment of the present invention, the delay time degradation rates of the intermediate transistors are ignored and only the delay degradation rates of the transistors connected to the input and the output pin in each logic block are counted. For example, if the delay time degradation rate, δ_{in}, is ten percent (.1) of the transistor connected directly to the input pin and if a fresh transistor (no degradation) has a delay of 1 unit, then it is readily apparent that it will take a signal 1.1 units to pass an aged transistor.

In accordance with the exemplary, non-limiting embodiment of the present invention, when a computer calculates the delay time of an *aged* circuit, only the degradation rates of the transistors directly connected to the input pins and the output pins are taken into account, whereas the degradation rate of other transistors are ignored. In other words, the delay time is adjusted only by the delay time degradation rates of the transistors connected to the input and output pins only.

That is, the delay time of an aged circuit is equivalent to the delay time of the fresh circuit plus the additional delay caused by the degradation of the transistors connected to the input pin and the output pin. To obtain this additional delay time, the delay degradation rate (*e.g.*, δ_{in}) should be multiplied by a ratio (*e.g.*, λ_{IN}). This ratio provides the delay caused by this particular transistor to the entire delay time (*e.g.* the delay time between the input pin and the output pin). That is, ($\delta_{in} * \lambda_{IN}$) is the additional time to be added to the delay time of the fresh circuit.

As is consistent with the exemplary embodiment of the present invention, there are instances when the degradation is insignificant and is not included in the adjusted delay time. For example, the time degradation rate is insignificant when the N-channel transistor is not activated, when the signal changes from high level to low level. In these instances, the ratio will be 0 since the degradation delay time in this instance should be ignored.

To facilitate understanding of the λ, consider the example on pages 19-20 of the specification. A logic block has three stage inverters. Each stage inverter has the same delay time as the other stage inverters. In other words, it does not matter whether the N-channel transistor is turned on or off, the delay time will always be the same. For example, in an inverter which has a n-channel transistor and a p-channel transistor, when the n-channel transistor is turned off, the p-channel transistor may be turned on causing the delay.

Regardless of whether the inverter has a p-channel transistor or not, the delay of each inverter is the same (for example, the delay of each inverter may equal to 1; then the total delay of a three stage inverter will always be 3 even if in the first stage, the N channel transistor is turned on, in the second stage the P-channel transistor is turned on and in the third stage the N-channel transistor is turned on). As a result, when the signal turns from low level to high level in the transistor connected to the input pin, $\lambda = 1/3$ (delay of the first stage inverter over the delay of the entire block). There are instances, however, when the degradation rate is too insignificant such as when the input of the transistor connected to the input pin changes from high level to low level (N-channel transistor is not activated), as such λ will be 0. In short, when the degradation

rate is insignificant and should not be taken into account in calculating the total delay of the aged circuit, λ will be 0.

These general remarks are provided by way of an example only to facilitate the understanding of the exemplary embodiments of the present invention and are not to be construed to limit the scope of the claims. Next, Applicant respectfully addresses the rejections.

Connection by a Computer

The Examiner rejected claims 3-6 and 9-12 because the Specification was amended to recite "in a computer" as opposed to "by a computer" and because it is unclear how the logical blocks would be connected by a computer (see pages 3 and 5 of the Office Action). Applicant respectfully submits that the Specification has been amended to remove the objected terminology of "connected by a computer" or "connected in a computer." Moreover, the specification clearly discloses one conventional way of connecting the logic blocks to each other via wire, for example (see page 20 of the specification).

Therefore, it is now appropriate and necessary for the Examiner to withdraw this rejection of claims 3-6 and 9-12.

Rejected Terminology in the Claims

The Examiner rejected claims 2, 4, 8-10, and 13 for allegedly reciting subject matter not described in the specification. In particular, claims 2, 8, and 13 for defining the plurality of V_c, claims 4 and 10 for containing "ratios of delay time degradations," and claim 9 for reciting "one

of". Applicant respectfully disagrees with the Examiner. For the sake of expediting prosecution, however, Applicant amends claims 2, 4, 8, 10, and 13. Furthermore, these rejections are traversed in view of the following remarks.

1. Claims 2, 8, and 13

Claims 2, 8, and 13 have been amended to further clarify the invention. In particular, the claims are directed to calculating a circuit property of a logic level circuit , for example, a delay time of a fresh circuit (V_A) and a delay time of an aged circuit (a degraded V_A). In particular, a block property of a logic block (V_B) which is included in the logic circuit is calculated. The block property can be a delay time of a logic block, which is calculated using a number of transistor properties (V_C), which are properties of various transistors in the logic block. V_C may be a delay time of a particular transistor. Then using the calculated V_B, the V_A (delay time of a fresh circuit) is calculated. To determine a degraded V_A (delay time of an aged circuit), delay degradation time of a first V_C and a second V_C is calculated. These two V_C values are the delay time of a transistor connected directly to the input pin and a transistor connected directly to the output pin. The aged delay time (V_A) is calculated by adjusting the delay time of a fresh circuit by the calculated degradation delay time.

These recitations of claims 2, 8, and 13, are fully supported on pages 8-12 of the Specification. In view of these amended claims 2, 8, and 13, it is appropriate and necessary for the Examiner to now withdraw this rejection of the claims.

II. Claims 4 and 10

Claims 4 and 10 have been rewritten to remove the previously added term "degradations". Applicant therefore respectfully requests the Examiner to withdraw this rejection to the claims.

III. Claim 9

Claim 9 recites: "calculating variations of signal delay times caused by aging based on transistor property values only for transistors inside the logic block connected directly to one of the input pin and the output pin of the logic blocks." The Examiner alleges that the recitation "one of" has no support in the Specification. Applicant respectfully disagrees.

For example, the originally filed Fig. 1, shows an exemplary transistors 211 and 221, where the transistor 211 is connected only to the input pin and where the transistor 221 is connected only to the output pin. Similarly, the original claim 2 recited "transistor connected to an input pin" and "a transistor connected to the output pin". Moreover, pages 8-9 of the specification describe that one exemplary technique of obtaining accurate delay time calculation at a small amount of time is to calculate the effect of hot electron only in connection with a transistor at the input pin and a transistor at the output pin, where N-channel transistors in the part shown by a question mark "?" (the middle transistors) are ignored. Since the specification clearly discloses a logic block with a number of transistors and one transistor being connected to the input pin only and another transistor being connected to the output pin only, the recitation of

having a transistor connected to an input or an output pin is clearly supported by the specification.

It is appropriate and necessary for the Examiner to withdraw this rejection and to consider claim 9 on the merits.

Ratios of Delay Time Degradations

The Examiner alleges that one of ordinary skill in the art would not be enabled without undue experimentation why the value of the λ is not ½ when in the middle stage the input changes from high level to low level with zero delay (see pages 6-7 of the Office Action). Applicant respectfully disagrees. In general, Applicant respectfully points to the general remarks, which are applicable with equal force herein.

Moreover, Applicant respectfully turns to the disclosure of a three stage inverter, where the delay of each stage is equal. In other words, each stage has a delay of 1 regardless of whether the N-ch transistor is turned on or off. This is possible because when the N-ch transistor is turned off, a P-ch transistor could be functioning and causing the delay. As a result, the total delay time of a three stage transistor is 1+1+1 = 3, *e.g.*, Tpd1n0 + Tpd2p0 + Tpd3n0.

However, since in the illustrative embodiment, the degradation rate is significant only when the N-ch transistor is turned to ON, the ratio of delay times will be 0 for all other times. In short, the degradation delay time of a transistor connected to the input pin and of a transistor connected to the output pin is disregarded at all times except when the N-ch transistor is turned on. Therefore, it would have been apparent to one of ordinary skill in the art that the λ of three

stage inverter is one third or zero and the λ of a four stage inverter is one fourth or zero. In short, the delay degradation rate is either counted or not. Since, it is readily apparent why the ratio is 1/3 and not ½ for a three stage inverter, Applicant respectfully requests the Examiner to withdraw this rejection to the claims.

Rejections under 35 U.S.C. § 103(a)

Claims 2, 3, 5, 8, 9, 11, 13, and 14 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,047,247 to Iwanishi et al. (hereinafter "Iwanishi") in view of U.S. Patent No. 6,278,964 to Fang et al. (hereinafter "Fang"). Applicant respectfully traverses this rejection and respectfully requests the Examiner to reconsider in view of the following comments. Applicant respectfully incorporates by reference arguments submitted in the Amendment under 37 C.F.R. § 1.111 on December 2, 2003.

Independent claim 2, among a number of unique features requires "wherein only the first V_C and the second V_C are used in calculating degradation delay and wherein a degraded V_A is calculated from the V_A and the calculated degradation delay." The Examiner acknowledges that Iwanishi does not disclose or suggest a V_C value representing a transistor property. The Examiner, however, alleges that Iwanishi discloses calculating a cell property based on "circuit information," and that Fang discloses a hot-carrier effect calculation based on circuit information including device parameters of all elements of a circuit. The Examiner further alleges that if a cell comprised only a single inverter, the inverter would then be connected directly to an input pin of the cell and an output pin.

Applicant respectfully submits that Fang is no different from the prior art disclosed in Applicant's specification. *Assuming arguendo* that Fang teaches a single inverter, Fang still fails to teach or suggest using only the first V_C and the second V_C in calculating an aged circuit delay. If only one inverter existed than there would be no second V_C for calculating the degradation rate. In fact, in Fang's method, the alleged degradation will be calculated for every transistor, thereby requiring high amount of calculation. Fang does not teach or suggest calculating the degradation delay time for only the first and second V_C, where one is connected directly to an input pin and another is connected directly to an output pin. Further, as discussed in the previous Amendment, there would have been no suggestion or motivation for combining Iwanishi and Fang.

The Examiner alleges that the motivation would have been that Fang discloses in detail the circuit information. However, the Examiner does not explain why, without impermissible hindsight reconstruction, there would have been motivation to select from Fang any particular types of circuit information and combining them into Iwanishi to arrive at Applicant's invention.

In short, the combined teachings of Iwanishi and Fang fail to teach or suggest "wherein only the first V_C and the second V_C are used in calculating hot electron effect and wherein the circuit property of the logic level circuit is modified in accordance with the hot electron effect," as recited in claim 2. For at least these exemplary reasons, Applicant respectfully submits that it is appropriate and necessary for the Examiner to withdraw this rejection of claim 2.

Independent claims 3, 8, 9, and 13 recite features similar to the features argued above with respect to claim 2. Since independent claims 3, 8, 9, and 13 contain features that are similar to the features argued above with respect to claim 2, those arguments are respectfully submitted to apply with equal force here. For at least substantially the same exemplary reasons, therefore, Applicants respectfully request the Examiner to withdraw this rejection of independent claims 3, 8, 9, and 13 and their dependent claims 5, 11 and 14.

Allowable Subject Matter

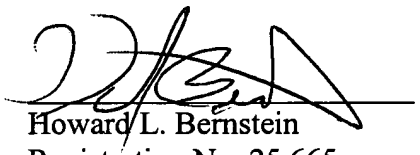
Applicant thanks the Examiner for indicating that claims 4, 6, 10, and 12 contain allowable subject matter. It is respectfully submitted that this Amendment overcomes the rejections under 35 U.S.C. § 112, first paragraph. Applicant, therefore, respectfully requests the Examiner to indicate allowance of these claims.

Conclusion and request for telephone interview

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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CUSTOMER NUMBER

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